ABSTRACT

The growing demand for computational power has pushed the research and development of digital processors that are even more dense in terms of transistor number and faster clock rate, without ignoring concerning constraints such as energy consumption, heat dissipation, manufacturing complexity and final market costs. Another approach to deal with digital information is quantum computation, that relies on a basic storage entity that keeps a superposition of the two possible states, in contrast with of a bit of a conventional computer, that stores only one of these two states. Simulators for quantum computation can run quantum algorithms on conventional computers. However, since these are developed using a software implementation, performance limitation occur due to the classical computational model used. This dissertation presents an implementable hardware architecture of a specialized coprocessor that simulates quantum operations, employing an application-specific design that allows parallel processing based on component replication and pipelining. The proposed architecture includes a quantum state memory, where individual and joined states of *q-bits* are stored; a scratch memory, dedicated to storing quantum operators that are built at runtime; the arithmetic unit, that performs complex numbers multiplications, to allow the full computation of tensorial and scalar products of matrices, required to implement quantum operators; the measurement unit, that is required to perform quantum state observation; and the control unit, that controls proper operation of the datapath components using a microprogram and some other auxiliary components.

Keywords: Coprocessor. Quantum computing. Emulators