ABSTRACT

In recent years, the theme of artificial neural networks (ANNs) has taken a relevant position in the area of intelligent systems. An ANN is a powerful resource to solve problems involving prediction, pattern recognition, optimization and control of servomechanisms, specially non-linear ones. Computationally, a neural network can be implemented in software or in hardware (or by both ones). This work proposes a hardware architecture to computing a multilayer neural network. Solutions in hardware are often faster (more efficient) than solutions in software. A neural network is a favorable field to the use of parallelism, wherein several artificial neurons can be computed simultaneously. This Project, well as exploring parallelism, allows the topology of the neural network to be configurable, i.e., hardware supports changes (*on-the-fly*) of the number of inputs, number of layers and neurons per layer. Thus, many applications of ANNs can be implemented in the proposed hardware. In order to reducing the processing time of arithmetic operations, the notation of IEEE-754 *floating-point* is not used, and a real number is represented as a *fraction of integers*. So, arithmetic operations are limited to integer operations, performed by combinational circuits. A simple state machine is demanded to computing sums and products using fractions. The activation function of the neuron is computed using arithmetics – a *Lookup Table* is not used in this project. Two theorems are proposed to ground the arithmetic strategy in the activation function computation. In addition, the sigmoidal activation function is computed by polynomials, whose operations are sums and products. Thus, the arithmetic circuit of the neuron weighted sum is reused to compute the sigmoid – this decreases the total area of the circuit. The final results of the neural system simulation validated the proposed architecture and the next step, therefore, can be the *synthesis* of the hardware in FPGA.

Keywords: Artificial neural networks, hardware for neural networks, computational arithmetics, fraction of integers, activation function, sigmoid, parallelism.